1.1.1 Analog-digital systems

Studiengang	Elektro- und Informationstechnik (Master)
Modulname	EITM220I Analog-digital Systems
Zugeordnete Lehrveranstaltungen	EITM221I Analog-digital Systems EITM222I Test of Digital Systems
Studiensemester	2nd Semester
Modulverantwortlicher	Prof. Dr. Rudolf Koblitz
Dozenten	Prof. Dr. Rudolf Koblitz Prof. Dr. Gerhard Schäfer
Sprache	English or German; the course language will be announced at the beginning of the semester
Lehrform, SWS und Gruppengröße	Courses, 2h+2h/week
Modus	Mandatory in the study field Information technology, elective in the other study fields of the program
Turnus	Summer semester
Arbeitsaufwand	On-campus program 60 h, self study 90 h
Kreditpunkte	5 CP
Empfohlene Vorkenntnisse	Digital Circuit Design, Electronics, feedback control systems
Voraussetzungen nach Prüfungsordnung	none
Lernziele / Kompetenzen	*Allgemein:* Modern system design covers the synthesis of analogue and/or digital functional blocks and the final verification of the complete system not only in the design process. Basic skills in digital and analogue system design are extended to testing aspects and mixed signal applications. Fault effects in both analogue and digital systems are presented as well as according fault models and test strategies. Description and simulation methods related to mixed signal systems are discussed on different important phase locked loop circuits. *Zusammenhänge / Abgrenzung zu anderen Modulen:* The components of a digital system and the according design methods should be well known. It is set as entry requirements. *Kenntnisse, Fertigkeiten, Kompetenzen:* Upon successful completion the students, • are able to describe mixed analogue digital circuits in time and frequency domain • can apply the simulation programs for behavioral analysis • can interpret the simulation results in time-domain as well as in a phase representation • can describe especially a PLL by its parameters • will be able to distinguish the block function by different realizations alternatives (e.g. phase comparators) • know the effects of fault models in analogue and digital systems • are able to verify the testability of digital circuits (Design for Testability DFT) • know the application of test pattern generation procedures • can apply boundary scan techniques • are able to use standard build in self-test methods

Inhalt	*Analog-digital Systems* • basics of PLL • comprehensive view of the different phase-comparators • Representation in the time-domain and in the phase plane • acquisition Behaviour of PLL's • Noise in PLL Systems • Applications of PLL as Frequency-Synthesis, Lock-in-detector, Costas-Loop • Fully digital PLL's • Waveform generation via Direct Digital Synthesis (DDS) *Test of digital systems* • Testenvironment • Fault models • Fault simulation • Automatic testpattern generation • Build in self test • Scan path techniques • Boundary scan • Test of special structures (e.g. RAM, ROM)
Studien- und Prüfungsleistungen	Assessment is done by either for both lectures common, a written exam (90 minutes) or an oral examination (20 minutes). The form of examination will be announced at the beginning of the semester.
Medienformen	• course manuscript • slides (Powerpoint, PDF) • Boundary scan training program • Exercises • Simulation with SPICE embedded in the Lecture (EITM221I)
Literatur	Wojtkowiak, Hans: *Test und Testbarkeit digitaler Schaltungen*, Teubner Verlag 1988 Wunderlich H.J*.: Hochintegrierte Schaltungen, Prüfgerechter Entwurf und Test*, Springer Verlag 1991 Jha N.,Gupta S: *Testing of Digital Systems*, Cambridge University Press, 2003 Parker K.P.: *The Boundary Scan Handbook,* Kluwer Academic Publisher, 2003 Floyd Gardner: *Phaselock Techniques*, Wiley & Sons, Edition: 3rd ed. (Aug., 16.2005) ISBN 978-0471430636 Roland Best: *Theorie und Anwendung des Phase-locked Loops*, AT-Verlag Aarau (Switzerland). 4.Auflage 1987 , ISBN 3-85502-132-5 P.V.Brennan: *Phase-Locked Loops: Principles and Practice*, McGraw-Hill 1996, ISBN 0-07-007568-9 (First published by MACMILLAN PRESS LTD William C.Lindsey, Marvin K.Simon*: Phase-Locked Loops And Their Application*, IEEE Press, 1978, John Wiley\&sons Wiley Order number: 0-471-04175-0, IEEE International Standard Book-#: 0-87942-101-0